New Claims

1. Phase detector for a phase-locked loop for didgital input signals in which the digital summed value for a particular number of bits is equivalent to Zero, said phase detector having a sampled and digitized data signal supplied to it, having a delay stage (52) for delaying the data signal by one or more sampling clock periods, having a subtraction stage (53), to which the undelayed and the delayed data signal are supplied, and comprising a filter or control stage (60), to which the output of the subtraction stage (53) are supplied at whose output the phase error can be tapped off, **characterized in that** a processing stage (54) is provided, located between the substraction stage and the filter or control stage (60), which assigns one of a plurality of possible output values, to the respective differential value, wherein the full differential value range is subdivided in a number of sub-ranges corresponding to the plurality of possible values, so that all differential values in one of the sub-ranges will get the same output value assigned.

2. Phase detector according to Claim 1, wherein the substraction stage is integrated in a comparison stage which compares the delayed sample with said undelayed sample and assigns said one of a plurality of output values to the respective differential value.

3. Phase detector according to Claim 1 or 2, wherein said control stage (60) is a PI controller.

4. Phase detector according to one of Claims 1 to 3, in which the delayed digital sample is deducted from the undelayed digital sample in the subtraction stage (53) in each case.

5. Phase detector according to one of Claims 1 to 4, in which a rectifier (51) for signal conditioning is

provided which has the sampled and digitized data signal supplied to it, the data signal being a ternary data signal, in particular.

6. Phase detector according to Claim 5, in which the sampled and digitized ternary data signal is supplied, before rectification, to a separating stage (55) in which the data signal is separated into a positive and a negative path.

7. Phase detector according to Claim 6, in which separate delay, subtraction and processing stages (52, 53, 54) or delay (52) and comparison stages are provided for each path, and in which an addition stage (56) is provided in which the assigned output values from the processing (54) or comparison stages are added and, combined in this way, are passed on to the filter or control stage (60).

8. Phase detector according to Claim 7, in which, in addition to the separate delay, subtraction and processing stages (52, 53, 54) or delay (52) and comparison stages for the positive and the negative path, there are also separate delay, subtraction and processing stages (52, 53, 54) or delay (52) and comparison stages for a further path, in which the complete data signal, including the positive and the negative path, is processed, the output values assigned by the processing stages (54) or comparison stages likewise being supplied to the addition stage (56).

9. Use of the phase detector according to one of Claims 1 to 8 in a phase-locked loop to recover the data clock signal for a digital signal.

10. Use according to Claim 9, the sampling clock signal for sampling the data signal corresponding to the data clock signal in the data signal.

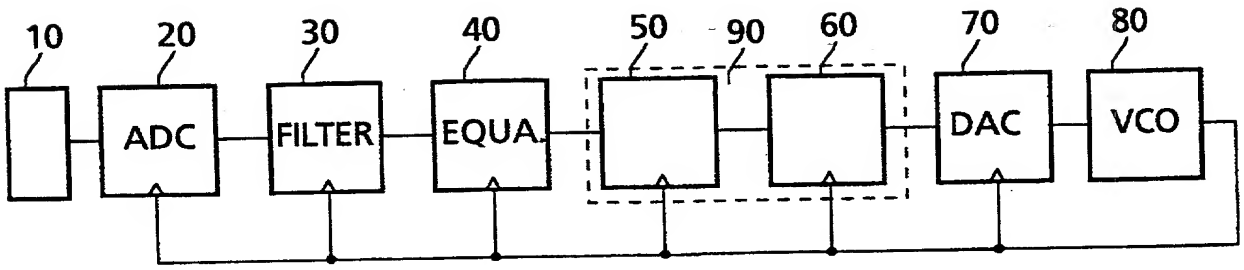
10
20
30
40
50
90
60
70
80
ADC
FILTER
EQUA.
DAC
VCO

Fig.1

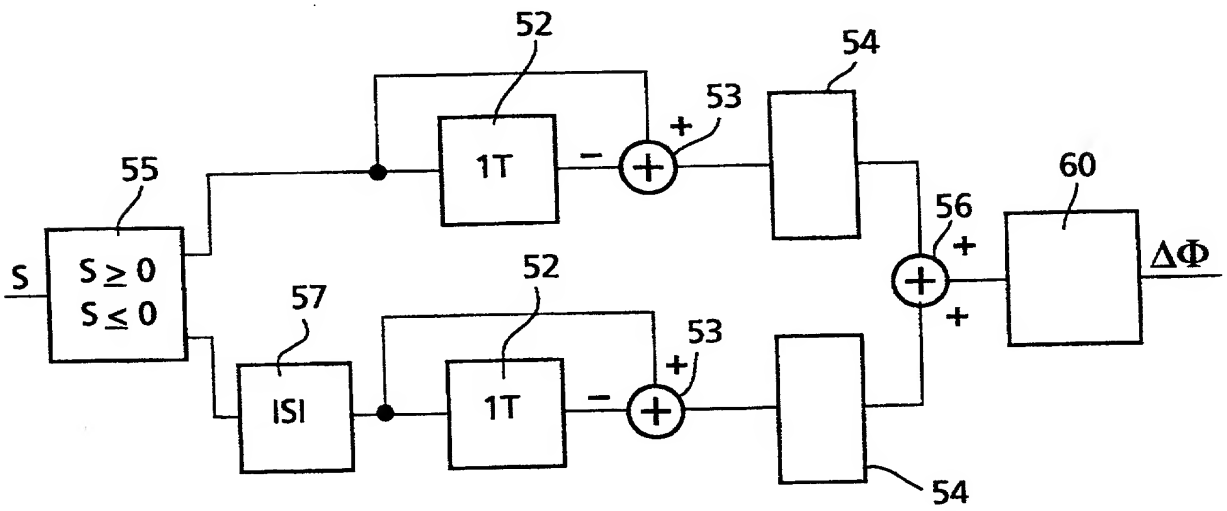
52
54
53
55
1T
60
56
S
S ≥ 0
S ≤ 0
ΔΦ
57
52
53
ISI
1T
54

Fig.4

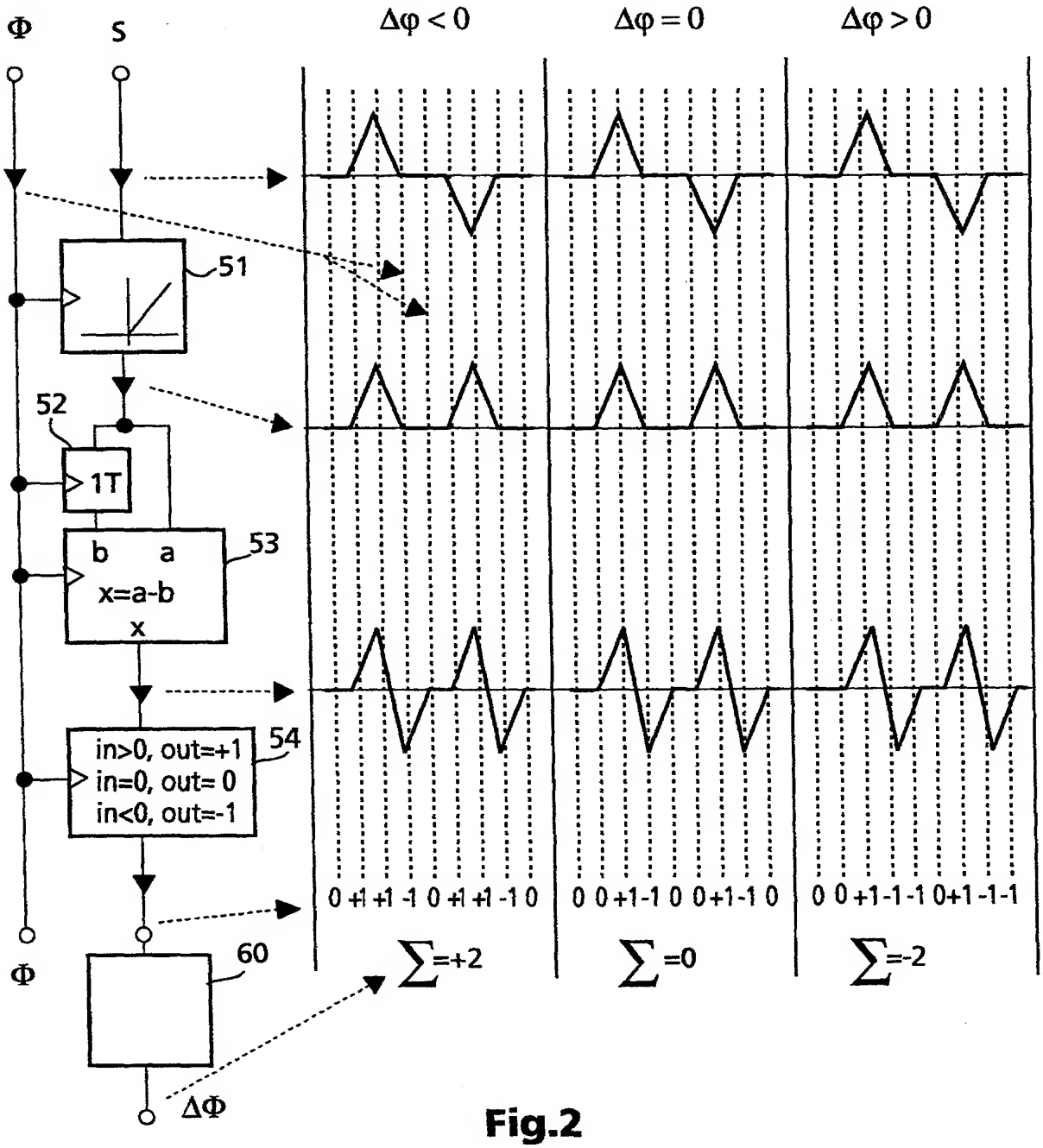
Φ
S
Δφ < 0
Δφ = 0
Δφ > 0
51
52
1T
53
b a
x=a-b
x
54
in>0, out=+1
in=0, out= 0
in<0, out=-1
0 +1 +1 -1 0 +1 +1 -1 0
0 0 +1 -1 0 0 +1 -1 0
0 0 +1 -1 -1 0 +1 -1 -1
Σ=+2
Σ=0
Σ=-2
Φ
60
ΔΦ

Fig.2

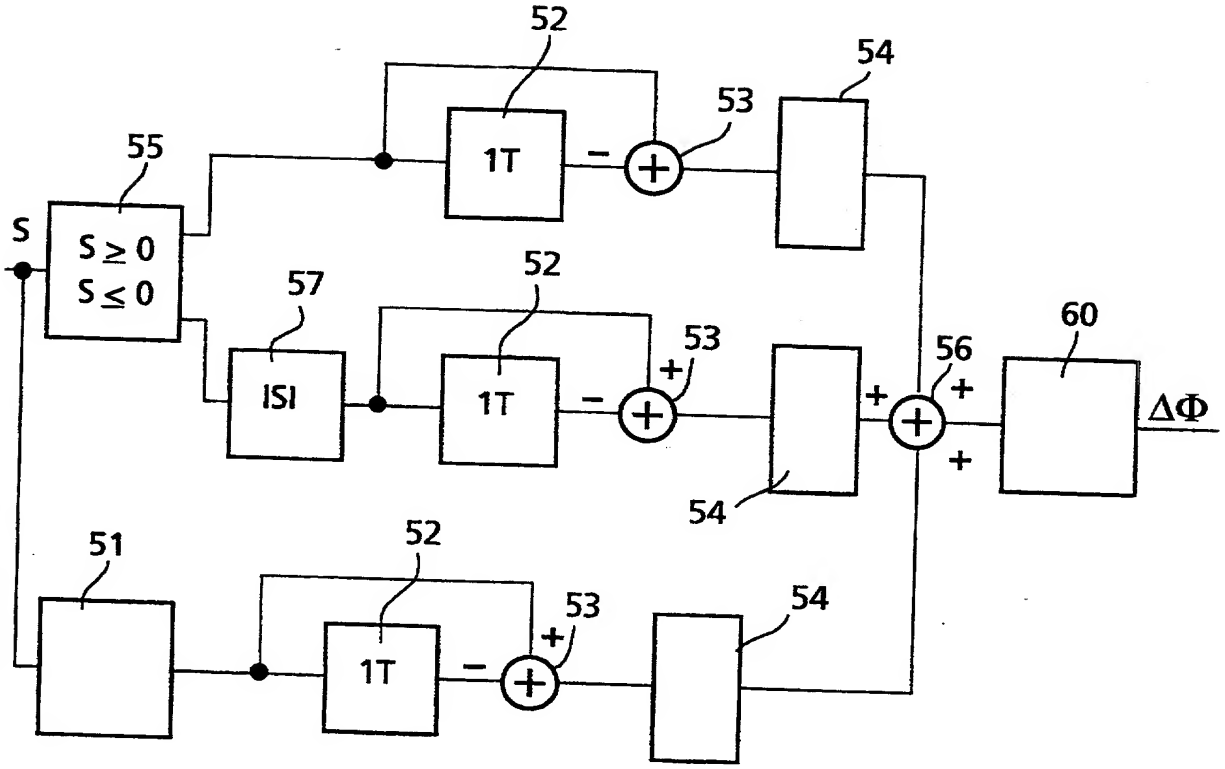
52
54
53
55
1T
S
S ≥ 0
S ≤ 0
57
52
53
56
60
ISI
1T
ΔΦ
54
51
52
53
54
1T

Fig.5

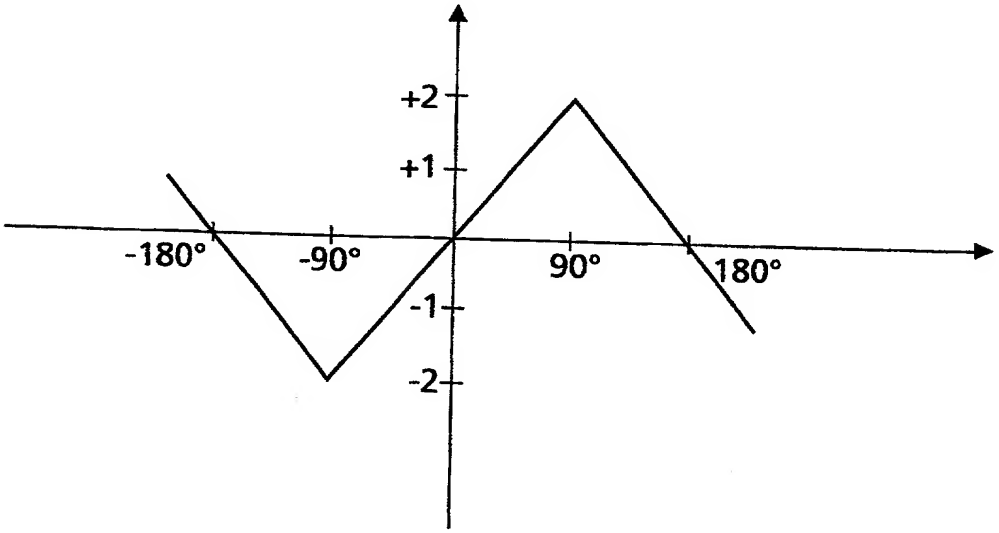
+2
+1
-180°
-90°
90°
180°
-1
-2

Fig.3

EXPRESS EL 902324433 US

PD990053

DECLARATION FOR UNITED STATES PATENT APPLICATION,
POWER OF ATTORNEY, DESIGNATION OF CORRESPONDENCE ADDRESS

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PHASE DETECTOR FOR A PHASE-LOCKED LOOP

the specification of which
(CHECK ONE) ( ) is attached hereto.
(xx) was filed on August 18, 2000, Application Serial. No. PCT/EP 00/08064 and was amended on .

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

I hereby claim foreign priority benefits under 35 USC 119 of any foreign application(s) for patent, utility model, design or inventor's certificate having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Date Filed	Yes	No
19941445.9	DE	August 30, 1999	xx	

I hereby claim the benefit under 35 USC 120 of any US Application(s) listed below, and, insofar as the subject matter of each of the claims of this Application is not disclosed in the prior US application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

Serial No.: Filed:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under of 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Joseph S. Tripoli (Reg. No. 26,040) Telephone: (609) 734-9443.

Address all correspondence to Joseph S. Tripoli, Patent Operations - Thomson multimedia Licensing, Inc. - CN 5312 - Princeton, New Jersey 08543-0028.

Signature: E. Wursthorn Date: 30 day of January ,2002.
Sole or First Joint Inventor: Edgar Wursthorn
Citizenship: DE
Residence and Post Office Address: Friedrichstr. 44/1
D-78073 Bad Dürrheim
Germany

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